REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change V_{OL2}, 0.5 V from min to max column. Change I_{01} test conditions: V_{CC} from 4.5 V to 5.5 V. Correct truth table input heading from A_1 to A_i. Change vendor part number on page 12. Editorial changes throughout.	87-01-15	Charles Reusing
B	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	02-06-10	Raymond Monnin

Current CAGE code is 67268

The original first sheet of this drawing has been replaced.

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY
David W. Queenan

CHECKED BY
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APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
86-10-01

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, BIPOLAR, QUAD BUS TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-86714**

SHEET 1 OF 11

DSCC FORM 2233
APR 97

5962-E110-02

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86714	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2917A	Quad three-state bus transceiver with interface logic

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat
2	CQCC1-N20	20	Square chip carrier

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.24 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case R	25°C/W
Case S	20°C/W
Case 2	20°C/W
Junction temperature (T_J)	+150°C
DC input current	-30 mA to +5.0 mA
DC output current, into outputs (except bus)	-30 mA
DC output current, into bus	100 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Clock pulse width (high)	20 ns minimum
Setup time, A data inputs	15 ns minimum

1/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).

Hold time, A data inputs	8 ns minimum
Setup time, bus to latch enable	15 ns minimum
Hold time, bus to latch enable	6 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Bus low level output voltage	V_{OL1}	V_{CC} = 4.5 V, V_{IN} = 0.7 V or 2.0 V	I_{OL} = 24 mA	1, 2, 3	All		0.4	V
			I_{OL} = 48 mA	1, 2, 3	All		0.5	V
Receiver low level output voltage	V_{OL2}	V_{CC} = 4.5 V,	I_{OL} = 4.0 mA	1, 2, 3	All		0.4	V
		V_{IN} = 0.7 V or 2.0 V,	I_{OL} = 8.0 mA	1, 2, 3	All		0.45	V
		$\overline{BE}$ = 2.4 V	I_{OL} = 12.0 mA	1, 2, 3	All		0.5	V
Bus high level output voltage	V_{OH1}	V_{CC} = 4.5 V, V_{IN} = 0.7 V or 2.0 V, I_{OH} = -15 mA		1, 2, 3	All	2.4		V
Receiver high level output voltage	V_{OH2}	V_{CC} = 4.5 V, V_{IN} = 0.7 V or 2.0 V, $\overline{BE}$ = 2.4 V	I_{OH} = -1.0 mA	1, 2, 3	All	2.4		V
		V_{CC} = 5.0 V, I_{OH} = -100 µA		1, 2, 3	All	3.5		V
Parity high level output voltage	V_{OH3}	V_{CC} = 4.5 V, I_{OH} = -660 µA, V_{IN} = 7.0 V or 2.0 V		1, 2, 3	All	2.5		V
Bus leakage current (high impedance)	I_{01}	V_{CC} = 4.5 V,	V_{OUT} = 0.4 V	1, 2, 3	All		-200	µA
		Bus enable = 2.4 V	V_{OUT} = 2.4 V	1, 2, 3	All		50	µA
			V_{OUT} = 4.5 V	1, 2, 3	All		100	µA
Bus leakage current (power off)	I_{02}	V_{CC} = 0 V, V_{OUT} = 4.5 V		1, 2, 3	All	-15	100	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Short-circuit output current	I_{OS1}	V_{CC} = 5.5 V,	Bus	1, 2, 3	All	-50	-225	mA
	I_{OS2}	V_{OUT} = 0 V 1/	Receiver	1, 2, 3	All	-130	-130	mA
	I_{OS3}		Parity	1, 2, 3	All	-20	-100	mA
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3	All		-1.2	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$	1, 2, 3	All		-0.72	mA
			All other inputs	1, 2, 3	All		-0.36	mA
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1, 2, 3	All		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V		1, 2, 3	All		100	µA
Supply current	I_{CC}	V_{CC} = 5.5 V		1, 2, 3	All		95	mA
Off-state output current (receiver)	I_{OFF}	V_{CC} = 5.5 V	V_{OUT} = 2.4 V	1, 2, 3	All		50	µA
			V_{OUT} = 0.4 V	1, 2, 3	All		-50	µA
Functional tests		See 4.3.1c		7, 8	All			
Propagation delay time, driver clock (DRCP) to bus	t_{PLH1}	V_{CC} = 5.0 V ±10% C_L = 50 pF ±10%		9, 10, 11	All		36	ns
	t_{PHL1}	R_{L1} = 1 K Ω ±5% R_{L2} = 130 Ω ±5%		9, 10, 11	All		36	ns
Propagation delay time, bus to receiver output (latch enabled)	t_{PLH2}	V_{CC} = 5.0 V ±10% C_L = 15 pF ±10%		9, 10, 11	All		33	ns
	t_{PHL2}	R_{L1} = 5 K Ω ±5% R_{L2} = 2 K Ω ±5%		9, 10, 11	All		30	ns

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, latch enable to receiver output	t_{PLH3}	V_{CC} = 5.0 V ±10% C_L = 50 pF ±10% R_{L1} = 1.0 K Ω ±5% R_{L2} = 130 Ω ±5%	9, 10, 11	All		33	ns
	t_{PHL3}		9, 10, 11	All		30	ns
Propagation delay time, A data to odd parity out (driver enabled)	t_{PLH4}		9, 10, 11	All		46	ns
	t_{PHL4}		9, 10, 11	All		40	ns
Propagation delay time, bus to odd parity out (driver inhibit)	t_{PLH5}		9, 10, 11	All		36	ns
	t_{PHL5}		9, 10, 11	All		36	ns
Propagation delay time, latch enable to odd parity output	t_{PLH6}		9, 10, 11	All		36	ns
	t_{PHL6}		9, 10, 11	All		36	ns
Propagation delay time, bus enable to bus	t_{PZH1} t_{PZL1}	V_{CC} = 5.0 V ±10% C_L = 50 pF ±10% R_{L1} = 1 K Ω ±5% R_{L2} = 130 Ω ±5%	9, 10, 11	All		26	ns
	t_{PHZ1} t_{PZL1}		9, 10, 11	All		21	ns
Propagation delay time, output control to output	t_{PZH2} t_{PZL2}	V_{CC} = 5.0 V ±10% C_L = 15 pF ±10% R_{L1} = 5 K Ω ±5% R_{L2} = 2 K Ω ±5%	9, 10, 11	All		26	ns
	t_{PHZ2} t_{PZL2}	V_{CC} = 5.0 V ±10% C_L = 5 pF ±10% R_{L1} = 5 K Ω ±5% R_{L2} = 2 K Ω ±5%	9, 10, 11	All		26	ns

1/ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

Device types	01	01
Case outlines	R, S	2
Terminal number	Terminal symbols	
1	$\overline{RLE}$	$\overline{RLE}$
2	R_0	R_0
3	A_0	A_0
4	$\overline{BUS}_0$	$\overline{BUS}_0$
5	GND_1	GND_1
6	$\overline{BUS}_1$	$\overline{BUS}_1$
7	A_1	A_1
8	R_1	R_1
9	$\overline{BE}$	$\overline{BE}$
10	ODD	ODD
11	$\overline{OE}$	$\overline{OE}$
12	R_2	R_2
13	A_2	A_2
14	$\overline{BUS}_2$	$\overline{BUS}_2$
15	GND_2	GND_2
16	$\overline{BUS}_3$	$\overline{BUS}_3$
17	A_3	A_3
18	R_3	R_3
19	DRCP	DRCP
20	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Inputs					Internal to device		Bus	Output	Function
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X X	X X	H H	L L	L L	X X	L H	L H	H L	Driver output disable and receive data via bus input
X	X	X	H	X	X	NC	X	X	Latch received data
L H	↑ ↑	X X	X X	X X	L H	X X	X X	X X	Load driver register
X X	L H	X X	X X	X X	NC NC	X X	X X	X X	No driver clock restrictions
X X	X X	L L	X X	X X	L H	X X	H L	X X	Drive bus

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

$\overline{BE}$	Odd parity output
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

FIGURE 2. Truth tables.

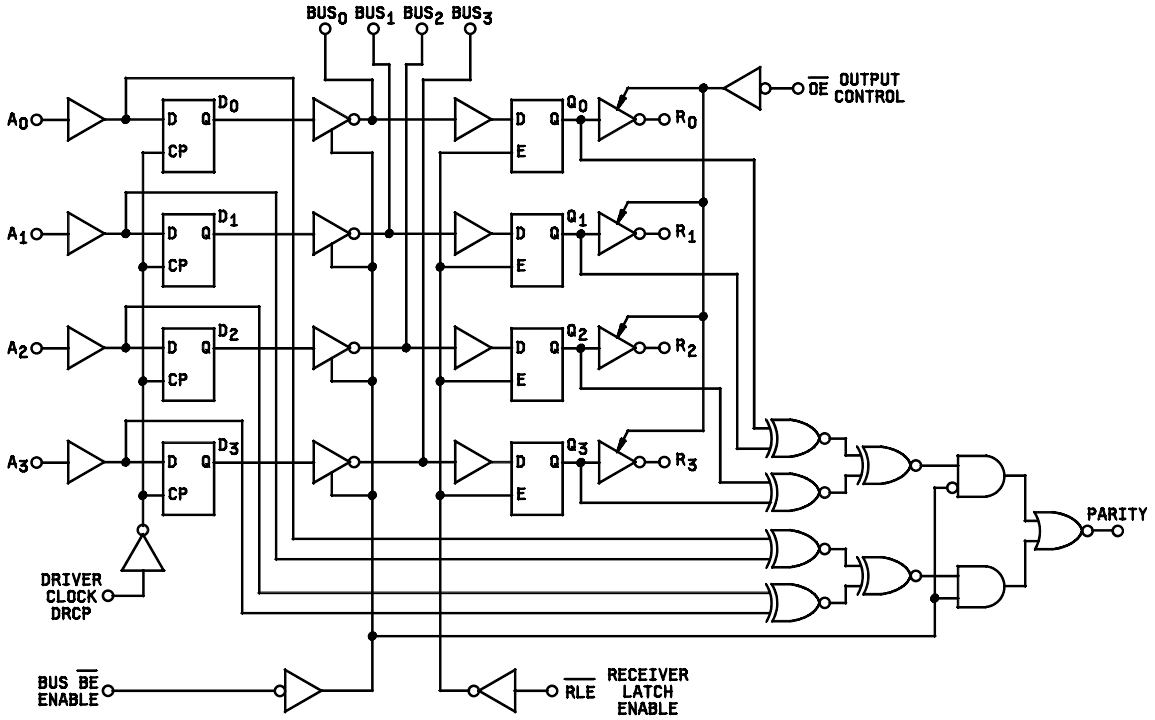

FIGURE 3. Logic diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-3851 and method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-06-10

Approved sources of supply for SMD 5962-86714 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 2/	Vendor CAGE number	Vendor similar PIN 1/
5962-8671401RA	3V146	2917A/BRA
5962-8671401SA	3V146	2917A/BSA
5962-86714012A	3V146	2917A/B2A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

Vendor CAGE number	Vendor name and address
3V146	ROCHESTER ELECTRONICS 10 Malcolm Hoyt Drive Newburyport, MA 01950